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FIRST NAMED INVENTOR APPLICATION NO. FILING DATE ATTORNEY DOCKET NO.]99/17/6,215 10722798 MAEDA 3057-2362-2**Y**

022850 MMC2/1002 OBLON SPIVAK MOCLELLAND MAYER % NEUSTADT FOURTH FLOOR 1755 JEFFERSON DAVIS HIGHWAY ARLINGTON VA 22202

EXAMINER CRANE, S ART UNIT PAPER NUMBER 2811

DATE MAILED:

10/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

,			
Advisory Action	Application No.	Applicant(s)	
	09/176,315	MAEDA ET AL.	
	Examiner	Art Unit	
	Sara W. Crane	2811	
The MAILING DATE of this communication app	pears on the cover sheet with the	correspondence add	lress
THE REPLY FILED 05 September 2001 FAILS TO PL Therefore, further action by the applicant is required to final rejection under 37 CFR 1.113 may only be either: condition for allowance; (2) a timely filed Notice of App Examination (RCE) in compliance with 37 CFR 1.114.	avoid abandonment of this appli (1) a timely filed amendment wh	cation. A proper relich places the application	ply to a cation in
PERIOD FOR R	REPLY [check either a) or b)]		
 a)	dvisory Action, or (2) the date set forth in the than SIX MONTHS from the mailing date of	of the final rejection.	
Extensions of time may be obtained under 37 CFR 1.136(a). The chave been filed is the date for purposes of determining the period of extension of the shorten (b) above, if checked. Any reply received by the Office later than three rearned patent term adjustment. See 37 CFR 1.704(b).	ension and the corresponding amount of the ed statutory period for reply originally set in	e fee. The appropriate ex the final Office action; or	tension fee under (2) as set forth in
1. A Notice of Appeal was filed on Appellan 37 CFR 1.192(a), or any extension thereof (37 C			
2. \square The proposed amendment(s) will not be entered	because:		
(a) \(\square\) they raise new issues that would require furt	ther consideration and/or search	(see NOTE below);	
(b) they raise the issue of new matter (see Note	e below);		
(c) they are not deemed to place the application issues for appeal; and/or	n in better form for appeal by ma	terially reducing or s	simplifying the
(d) they present additional claims without canc	eling a corresponding number of	finally rejected clair	ms.
NOTE:			
3. Applicant's reply has overcome the following reje	ection(s):		
4. Newly proposed or amended claim(s) wou canceling the non-allowable claim(s).	ld be allowable if submitted in a s	separate, timely file	d amendment
5. ☑ The a) ☐ affidavit, b) ☐ exhibit, or c) ☑ request to application in condition for allowance because:		sidered but does NO	OT place the
6. The affidavit or exhibit will NOT be considered be raised by the Examiner in the final rejection.	ibit will NOT be considered because it is not directed SOLELY to issues which were newly iner in the final rejection.		
	nt(s) a) will not be entered or b) will be entered and an would be rejected is provided below or appended.		
The status of the claim(s) is (or will be) as follows	s:		
Claim(s) allowed:			
Claim(s) objected to: 6-16 and 19			
Claim(s) rejected: <u>1-5 and 18</u> .			
Claim(s) withdrawn from consideration: 17 and 2	<u>o</u> .		
8. The proposed drawing correction filed on	is a)□ approved or b)□ disap	proved by the Exan	niner.
Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s)			

U.S. Patent and Trademark Office

10. Other: ____

Sara W. Crane
Primary Examiner
Art Unit: 2811

Continuation Sheet (PTO-303) 09/176,315

Continuation of 5. does NOT place the application in condition for allowance because: of reasons of record. Note that figure 3 of Chen et al. is a top view, where figure 1 is the cross-section 1-1. It is clear from figures 3 and 1 (as well as the discussion of column 3, lines 25-30 and 44-50) that the "p-Si" as shown in figure 1 is continuous in the body layer, and extends everywhere except directly under the source/drain regions. There is only one contact to the entire body layer, and that is contact 39. The body of transistor 26 in figure 1 is linked together with with the other FETs, so there is no need for more than one such contact (see column 3 as noted). Note that there is no "wiring part" shown in either of Chen figures 1 or 3 except for the gate electrode. Indeed, there is no other capacitance whatsoever shown coupled to the body layer except the gate capacitance, although the Chen teaching is to minimize the entire RC time constant, and not simply any one part of the RC time constant. Also, note that the amendment of 5 October 2000 deletes the frequency variable from claim 1, line 23. Even if the frequency variable is included, 1 divided by 500 MHz gives 2 nsec, and the Chen teaching is to have RC less than 1 nsec, so the claim limitation would be met in any case.